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08SCS21

(2)

Second Semester M.Tech Degree Examination, June-July 2009
Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Define computer Architecture with ISA and explain seven dimensions of ISA. **(08 Marks)**

b. What are the advantages of parallelism? With the performance result, explain the principle of locality and Amdahl's law? **(07 Marks)**

c. Suppose we have made the following measurements :
i) Frequency of FP operations = 25%
ii) Average CPI of FP operations = 4.0
iii) Average CPI of other instructions = 1.33
iv) Frequency of FPSQR = 2%
v) CPI of FPSQR = 20
Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5. Compare these two design alternatives using the processor performance equation. **(05 Marks)**

2 a. What are the different Fallacies and Pitfalls? Explain with example the various Fallacies and Pitfalls. **(08 Marks)**

b. What is pipelining? Explain the basics of RISC Instruction set with three classes of instructions? **(06 Marks)**

c. What are the different classes of pipeline hazards? Explain structural hazard with diagram. **(06 Marks)**

3 a. What is instruction level parallelism? Explain data dependency and control dependency with suitable example. **(08 Marks)**

b. Explain overcoming of data hazards with dynamic scheduling with examples. **(04 Marks)**

c. Explain dynamic scheduling using Tomasulo's approach using diagram. **(08 Marks)**

4 a. Explain with diagram the basic structure and its execution steps involved in instruction execution of a FP unit using Tomasulo's algorithm and extended to hardware speculation. **(10 Marks)**

b. Draw a neat diagram and explain branch target buffers with the steps involved in handling an instruction. **(06 Marks)**

c. Determine the total branch penalty for a branch-target buffer assuming the penalty cycles for individual mispredictions from table below :

Instruction in buffer	Prediction	Actual branch	Penalty cycles
Yes	taken	taken	0
Yes	taken	not taken	2
No		taken	2
No		not taken	0

Make the following assumptions about the prediction accuracy and hit rate :
i) Prediction accuracy is 90% (For instructions in the buffer).
ii) Hit rate in the buffer is 90% (For branches predicted taken). **(04 Marks)**

Explain limitations on ILP for realizable processors? **(05 Marks)**
Explain crosscutting issues in hardware versus software speculation. **(05 Marks)**
Explain Flynn's proposed model of categorizing all computers? Draw a basic structure of shared memory multiprocessor. **(10 Marks)**

What is multiprocessor cache coherence and explain basic scheme for enforcing coherence? **(08 Marks)**
Suppose you want to achieve a speedup of 80 with 100 processors, what fraction of the original computation can be sequential? **(06 Marks)**
Explain with diagram the limitations in symmetric shared-memory multiprocessors and snooping protocols. **(06 Marks)**

Explain any five advanced optimizations of cache performance. **(10 Marks)**
Explain protections in virtual memory and virtual machines. **(10 Marks)**

Draw a dataflow for computing cosx. Explain static vs dynamic dataflow. **(10 Marks)**
Explain VLIW architecture and pipe ling in VLIW processor with suitable diagram. **(10 Marks)**

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